GALILEO Timing Receiver

The Space Technology GALILEO Timing Receiver is a triple carrier single channel high tracking performances Navigation receiver, specialized for Time and Frequency transfer application.
It is a core derivative of a multi-channel GNSS receiver developed originally for the GALILEO SIS ICD 12.0 standard. Current version of GALILEO Receiver core has been upgraded for the Timing Receiver implementation, to SIS ICD 13.2 for supporting the L1 CBOC extended mode and E6 carrier. The GALILEO Timing receiver for the E5 signal implements the AltBOC coherent demodulation. The design is based on COTS latest generation digital IF processor equipped with wideband ADC and DAC Board supported by an FPGA of the most recent generation and state of art CMOS geometry (CMOS 40 nm).

Receiver Assembling

The receiver can be provided in two different assembling formats:

- stand alone 19”-1U case
- rack mounted 3U/6U Board set

When used as standalone Unit the 19”-1U Receiver assembling is complete of AC-DC adapter, fan coolers and internal high quality reference oscillator.
Alternatively when used as set of rack mounted 3U/6U Board external reference oscillator and proper DC power supplying system and clock references must be provided.
For what concern the stand alone 19”-1U case assembled unit, Fig. 1 reports the front panel of the Timing Receiver case, while Fig. 2 reports the rear panel.

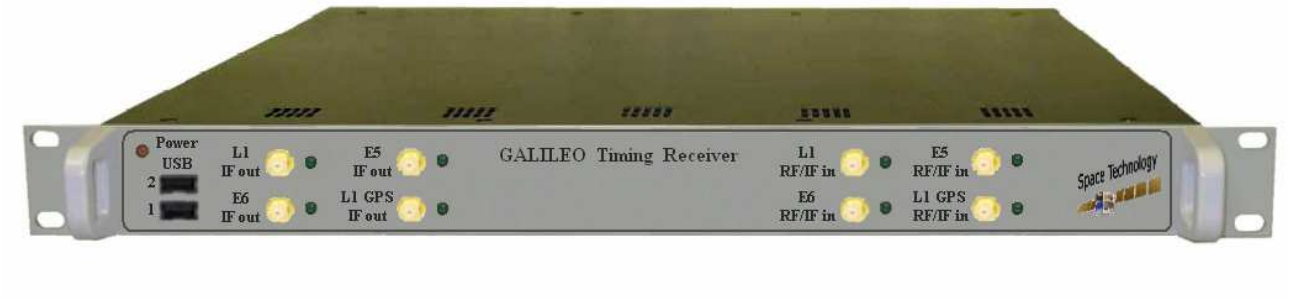

Fig. 1

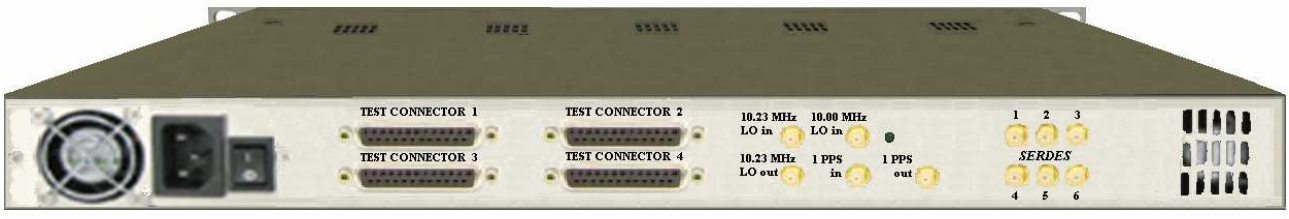

Fig. 2

Space Technology S.r.l.
Piazza Augusto Righi N. 8
(00146) Rome Italy
Contact: sales@spacetechnology.it
Phone: +39-06-55133935

For the rack mounted assembling solution, the number and type of Boards (3U/6U) will be described after the Factory Receiver configuration will be introduced (see Receiver Configurations Paragraph).

Receiver I/O interfaces

Fig. 3 reports a description of the interface provided by the Timing Receiver.

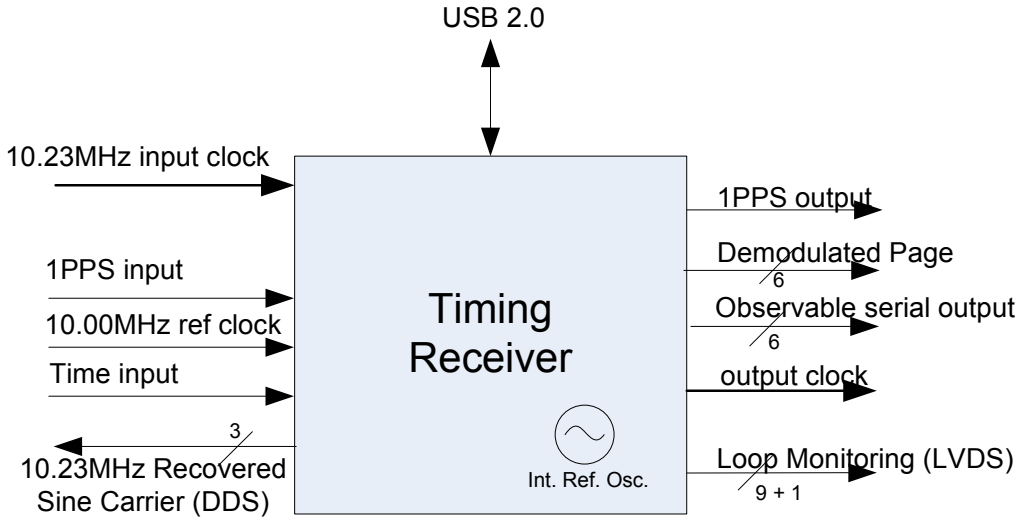

Fig. 3

The Timing Receiver is provided with a GUI aimed at configuring and monitoring the receiver using an external PC linked through a USB 2.0 interface channel.
Actually only one of the two foreseen USB interface is currently enabled.
A GPS L1 receiver module developed by Space Technology (and the associated configuration USB channel 2) is foreseen in the Timing Receiver product evolution, for supporting an accurate measurement and monitoring of the Galileo to GPS Offset Time (GGTO) or of the EGNOS to GPS Offset Time (EGTO) assuming an external Atomic Reference and a Time Event Counting measurement system with accuracy below 1 tenth of ns is provided externally to the Timing Receiver.

The monitoring interfaces are split in two main sections:

- an host PC interface section allowing to handle navigation algorithm with log data threads that are transmitted within 1PPS frame but that are floating w.r.t. the HW received 1PPS signal depending on the response of the SW.

Space Technology S.r.l.
Piazza Augusto Righi N. 8
(00146) Rome Italy
Contact: sales@spacetechnology.it
Phone: +39-06-55133935

- a real time interface aimed for accurate Time and Frequency implementation in which the main observable of the Timing Receiver are available on a set of digital line interfaces below described.

The following interface signals (Table 1) for clock and time measurement and receiver status monitoring are provided.

Signals	Panel	Description
L1-GAL RF/IF input	Front	L1-GAL Analog IF interface centered @143,22MHz (14·10.23MHz) or L1-GAL Analog RF interface centered @1575.420MHz depending on the purchased option
E5-GAL RF/IF input	Front	E5-GAL Analog IF interface centered @143,22MHz (14·10.23MHz) or E5-GAL Analog RF interface centered @1191.795MHz depending on the purchased option
E6-GAL RF/IF input	Front	E6-GAL Analog IF interface centered @143,22MHz (14·10.23MHz) or E6-GAL Analog RF interface centered @1278.750MHz depending on the purchased option
L1-GPS RF/IF input	Front	Currently not enabled
L1-GAL IF output	Front	L1-GAL IF @143,22MHz down converted monitoring output. Factory enabled only if any of the RF interface option is purchased.
E5-GAL IF output	Front	E5-GAL IF @143,22MHz down converted monitoring output. Factory enabled only if any of the RF interface option is purchased.
E6-GAL IF output	Front	E6-GAL IF @143,22MHz down converted monitoring output. Factory enabled only if any of the RF interface option is purchased.
L1-GAL IF output	Front	Currently not enabled
GAL USB 1 interface	Front	Monitoring PC interface USB 2.0
GPS USB 2 interface	Front	Currently not enabled
10.00MHz clock in	Rear	External 10.00MHz clock reference used when the receiver is SW configured to accept it to synchronize the internal 10.23MHz OCXO to an external time reference system.
10.23MHz clock in	Rear	External 10.23MHz clock reference used when the receiver is SW configured to accept it. It completely replace the internal 10.23MHz OCXO mostly for test and debugging purposes.
Output clock	Rear	Internal 10.23MHz OCXO clock reference. Such output will report in case either the external 10.00MHz or the internal 10.23MHz reference clock is selected, the output of the internal 10.23MHz OCXO. In case the external 10.23MHz will be selected and applied to the Timing Receiver, this signal will simply report a buffered replica of the external 10.23MHz input clock.
1 PPS input	Rear	This signal is the external 1PPS synchronization input. Is active high and it is supposed to be externally synchronous with the external 10.00MHz clock rising edge.
1 PPS output	Rear	This signal is the external 1 PPS synchronization output. It is active high and it is supposed to be internally synchronous with the OCXO 10.23MHz reference OCXO Oscillator.
Time serial input	Rear	It is a digital signal strobing synchronously with the 1 PPS strobe and the external 10.00MHz input clock the 32 bits of the GALILEO Receiver Time. Such a Time when not critical can be set via the USB link or being overwritten by one of the Demodulated Page Message fields (one of the three option is configurable via SW GUI).
Demodulated Page Messages (0 .. 5)	Rear	Digital Demodulated Page Message (0..5) representing in sequence L1A, L1B,E5A,E5B,E6A and E6B). Such signals are synchronous with the 1 PPS output going active 'High'(First Page Message bit) and with the rising edge of the output clock (first and all the Page Demodulated bits).

Space Technology S.r.l.
Piazza Augusto Righi N. 8
(00146) Rome Italy
Contact: sales@spacetechnology.it
Phone: +39-06-55133935

Observable Serial Output (0 .. 5)	Rear	Code phase offset, Carrier phase residual offset, Frequency residual offset, Start of Frame Offset, Fine code error are serially transmitted for each of the three GAL carrier using an enable strobe synchronously with the output clock
Loop Monitoring (0 .. 9)	Rear	DLL code error and PLL carrier phase error plus symbol clock for each of the three GAL carriers
10.23MHz recovered carriers (0..2)	Rear	10.23MHz sine carriers regenerated using the estimated carrier frequency error and a Direct Digital Synthesis technique applied to an internal dedicated NCO.
SERDES Monitoring(1..6)	Rear	These are 5Gbps links (each of the 6 SERDES output) aimed at monitoring at very high rate internal Receiver state variable. They require a receiver compatible with ALTERA Stratix 4 FPGA SERializer DESerializer interface. Therefore 10Gbps per carrier Monitoring could be allocated.

Table 1

Additional Test Connector pins could customized, upon request, using Test Connector 3 and 4.

Receiver Configurations

The receiver is a high quality acquisition and tracking receiver aimed for Ground Segment control of a GALILEO GNSS SV.

It allows acquiring and tracking a single SV because of the accuracy implied and the density of its real time output interfaces.

Therefore the Timing Receiver has been actually conceived as Ground Segment receiver for Down Link one way Frequency and Time Transfer implementation when properly driven by

- an external 10.00MHz Atomic Clock Reference
- an external and accurate Time Interval Counting machine with time resolution greater than the GALILEO system time

The receiver can be ordered with the following configuration:

- ***IF 143.22MHz input only***. This configuration is aimed at completely validating the Receiver when the SIS Generator does not provide the RF up-converter signal in L band but only analog IF signal in the 140MHz range domain (143.22MHz).
- ***RF instrumental input only***. This configuration is aimed at testing the Receiver when the SIS Generator provide the RF up-converter signal in L band at power level in the range from -20dBm down to -40dBm (i.e. much higher power level than SIS level guaranteed on Ground).

Space Technology S.r.l.
Piazza Augusto Righi N. 8
(00146) Rome Italy
Contact: sales@spacetechnology.it
Phone: +39-06-55133935

- ***RF antenna ready input only***. This configuration is aimed to test the Receiver when input signal is compliant with RF power levels guaranteed by GALILEO SIS on ground (in the range of -120dBm)

Fig. 1 and Fig. 2 reports the stand alone assembling for the complete solution up to RF antenna ready configuration.

For the Timing Receiver Rack Mounted version. according to which option is selected the following Boards will be needed:

- ***IF input only:*** Two digital IF 3U Boards each being of 3U form factor (1.0 6U slot)
- ***RF instrumental input:*** Two digital IF 3U Boards and 1 triple carrier receiver RF down converter. Each of them is based on a 3U form factor (1.5 6U slot)
- ***RF antenna ready input:*** Two digital IF 3U Boards and one 6U triple carrier antenna ready RF receiver and down converter. Each of them is based on a 3U form factor (2.0 6U slot)

In any case for the Rack Mounted version, independently from which version is purchased, the external clock references (for both Base Band and RF/IF front ends) shall be provided externally, together with proper DC power supplier (Voltage Current and Power Supply Ripple wise).

Main Functional & Performance characteristics

The main Functional and Performance characteristic are reported in Table 2.

Specification	Value	Note
Number of simultaneously Demodulated RF carrier	3	GALILEO L1, E5 and E6
Number of Demodulated Space Vehicles per carrier *)	1	Interface I/O limited see Note [1]
Minimum Acquisition C/N0	35dB-Hz	
RF Demodulator LNA Noise Figure	2.8 dB	
RF Front end without Antenna Noise Figure	3.2 dB	(0.4 dB filter & cables loss)
RF Front end without Antenna max Input signal, linear operation	-40 dBm	
RF Front end without Antenna absolute Max Input signal:	0 dBm	
Max RF Front gain end without Antenna Gain, (RF Input to BB analog out)	76.5 dB	47 dB RF Direct Demodulator +29.5 LNA & Filters
Analog AGC control range	30dB	+10dB – 20dB.
Noise level, BB analog output any channel (max gain) I,Q,I-,Q- (without Antenna Front End)	-46 dBm	@ 100 KHz BW
Noise level, BB analog output any channel (max gain) I,Q,I-,Q- (without Antenna Front End)	-19 dBm	wideband
Internal reference 10.23MHz OCXO	Y	Selectable via GUI
External synchronization to 10.23MHz LO	Y	Selectable via GUI
External synchronization to 10.00MHz LO	Y	Selectable via GUI

Space Technology S.r.l.
Piazza Augusto Righi N. 8
(00146) Rome Italy
Contact: sales@spacetechnology.it
Phone: +39-06-55133935

10.23MHz OCXO Integrated Phase Noise	0.0026 rad	Frequency integration interval [0.05 – 10E4] Hz (see Note [2])
RF Carrier Integrated Phase Noise	0.018 rad	Frequency integration interval [0.05 – 10E4] Hz
Digital AFC Loop BW programmable	Y	
Digital DLL Loop BW programmable	Y	
Digital PLL Loop BW programmable	Y	
Digital AFC Loop Order	First	
Digital DLL Loop Order	First	Carrier Aided
Digital PLL Loop BW programmable	Second	Coherent Phase Error Detector
Standard Deviation DLL Synchronizer error on AWGN channel @ 45dB-Hz	0.5 ns	BW = 0.05 Hz with Carrier Aiding being enabled and no dynamic stress error (still receiver)
Standard Deviation PLL Synchronizer error on AWGN channel @ 45dB-Hz	0.1 degree	BW = 0.1 Hz with *arctangent* coherent error detector and no dynamic stress error (still receiver)
Standard Deviation AFC+PLL Synchronizer error on AWGN channel @ 45dB-Hz	0.1Hz	BW = 0.1 Hz PLL second order with AFC disabled after PLL setting with arctangent coherent error detector and no dynamic stress error (still receiver)
PC Monitoring and Setting Interface	USB 2.0	Two USB interface are foreseen one for the GALILEO configuration and one for the GPS configuration. The GPS one is currently not enabled.
PC RX Monitoring and Setting GUI	Y	O.S. Window XP
PC RX Monitoring and Setting Driver	Y	.DLL file to be linked in Visual C++ (Windows XP)

Table 2

[1] *Natively it would be 12 per carrier. The Timing receiver limitation to single SV comes from the I/O real time interface connectors*

[2] *Below (Table 3) the Integrated Phase Noise calculation starting from a 10.00MHz OCXO low phase noise raw data (from OCXO data-sheet)*

INTEGRATED PHASE NOISE & JITTER

Offset Frequency (Hz)	Raw Data (dBc/Hz)	Anti-log of Raw Data	Apply Trapezoidal Rule
			Oscillator Frequency = 1,0000E+07 Hz
5,E-02	-44	3,98E-05	
1,E-01	-53	5,01E-06	1,12E-06
1,E+00	-90	1,00E-09	2,26E-06
1,E+01	-121	7,94E-13	4,50E-09
1,E+02	-145	3,16E-15	3,59E-11
1,E+03	-151	7,94E-16	1,78E-12
1,E+04	-152	6,31E-16	6,41E-12
			Phase Jitter: (Columns A-D)
			Integration = 3,381E-06
			Phi (rms rad) = 2,600E-03
			Phase Jitter (rms s) = 4,139E-11 This is the RMS phase jitter in seconds from the raw data

Table 3

Space Technology S.r.l.
Piazza Augusto Righi N. 8
(00146) Rome Italy
Contact: sales@spacetechnology.it
Phone: +39-06-55133935

Monitoring customization

The Timing Receiver is a fully observable receiver conceived with an internal Buffering system aimed at observing in Burst Mode (up to the Buffer saturation and then repeated in time after dumping on the Monitoring PC) via a SW GUI some of the internal design variable (I, Q demodulated symbols, Error variable for DLL, PLL and AFC etc.) or in real time (real time continuous) via parallel digital connector directly connected to an FPGA Base Band receiver Test Multiplexer. The Test Multiplexer can be controlled by the User via the Timing Receiver GUI. In some other specific cases, additional SQM (Signal Quality Monitoring) variable could be ad-hoc specified by the Customer, and directly implemented inside the FPGA Base Band Receiver, if they cannot be processed directly via SW elaboration due to the involved processing rate. As example of such customization below are reported the results of the RX tracking phase of L1B being observed internally to the FPGA, through the internal primary code accumulator signal. The Waveform below reported, is taken directly from Tektronix Logic Analyzer (LA) connected to the Digital Test Connectors 3 and 4 and ultimately to the FPGA Test Multiplexer.

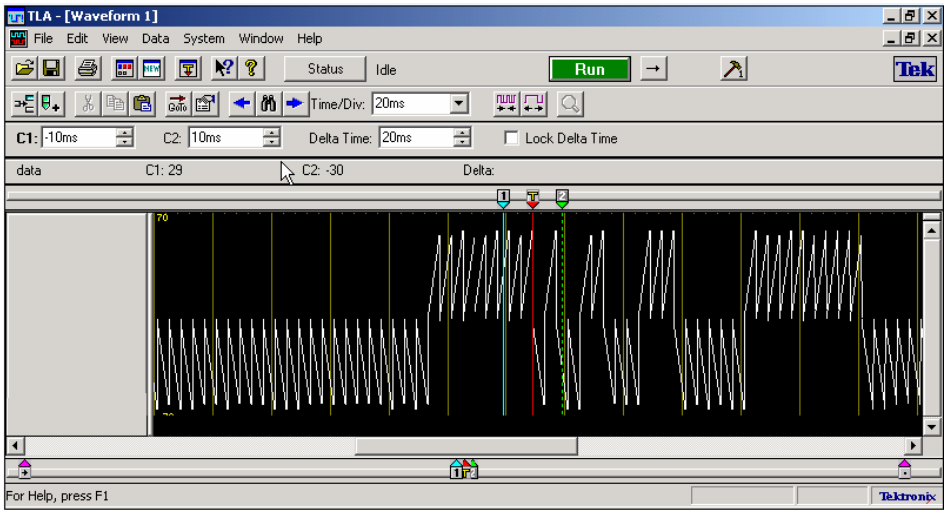

Fig. 4

Fig. 5 for example reports an acquisition (through Logic Analyzer during the Receiver tracking phase) of the FPGA internal L1B and L1C Despreader accumulator time evolution.

The top Logic Analyzer waveform in Fig. 5 shows the FPGA L1B (data channel) internal de-spreader accumulator, while the bottom waveform of Fig. 5 reports the L1C (pilot channel) despreader accumulator.

Note that in this case the code phase set by the Receiver is the same (like in a single DLL receiver) showing that L1B and L1C are fully synchronous and aligned.

Space Technology S.r.l.
Piazza Augusto Righi N. 8
(00146) Rome Italy
Contact: sales@spacetechnology.it
Phone: +39-06-55133935

As expected, the L1C pilot epoch is 25 times the L1B code epoch.

The Timing Receiver is equipped with a SW GUI (Fig. 7) capable of monitoring by time intervals: loop error signals, scattering diagram of the Demodulated symbols as well as to provide the Navigation message pages and their main decoded fields (Fig. 9), the CRC error (if any) plus the elapsed time.

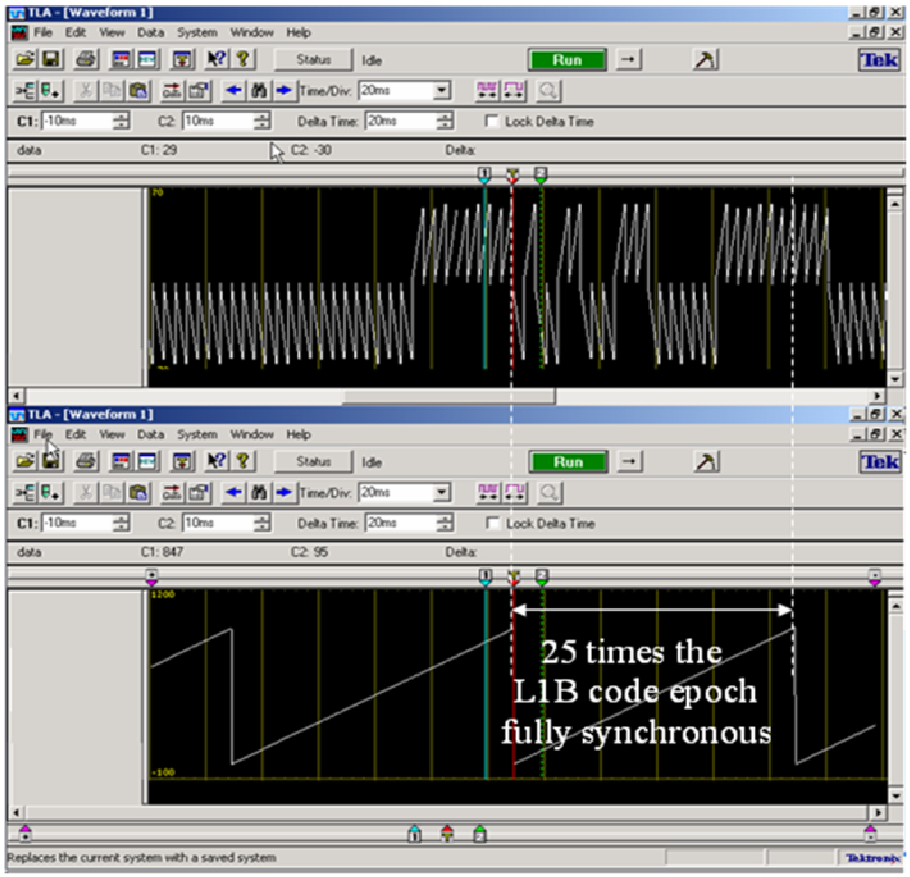

Fig. 5

Below in Fig. 6, the scattering diagram of L1B signal (I,Q) is shown after the symbol have been despreaded and carrier recovered.

Space Technology S.r.l.
Piazza Augusto Righi N. 8
(00146) Rome Italy
Contact: sales@spacetechnology.it
Phone: +39-06-55133935

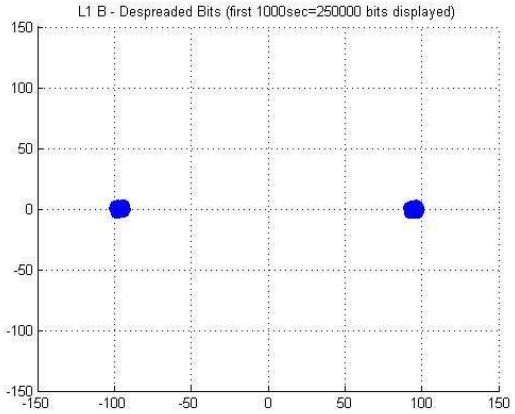

Fig. 6

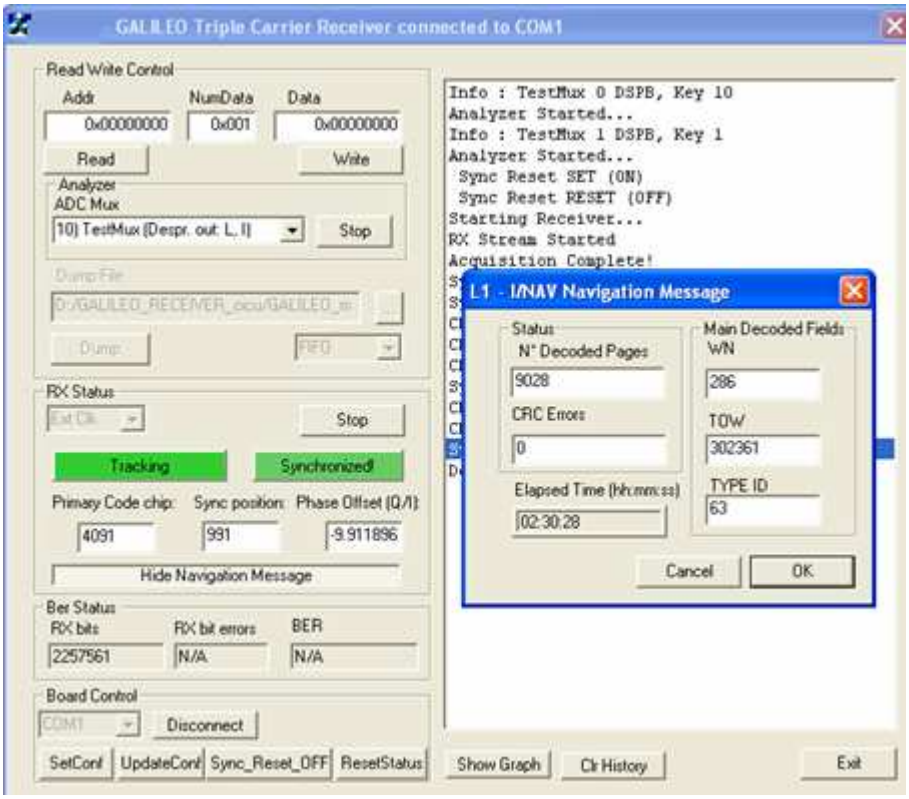

Fig. 7

Space Technology S.r.l.
Piazza Augusto Righi N. 8
(00146) Rome Italy
Contact: sales@spacetechnology.it
Phone: +39-06-55133935

It is also possible to appreciate the slight degradation introduced by the Timing Receiver RF front end comparing the L1B scattering diagram interfacing the receiver using a GALILEO SIS Generator at RF instrumental (not in the antenna ready mode) or at IF level. See Fig. 8.

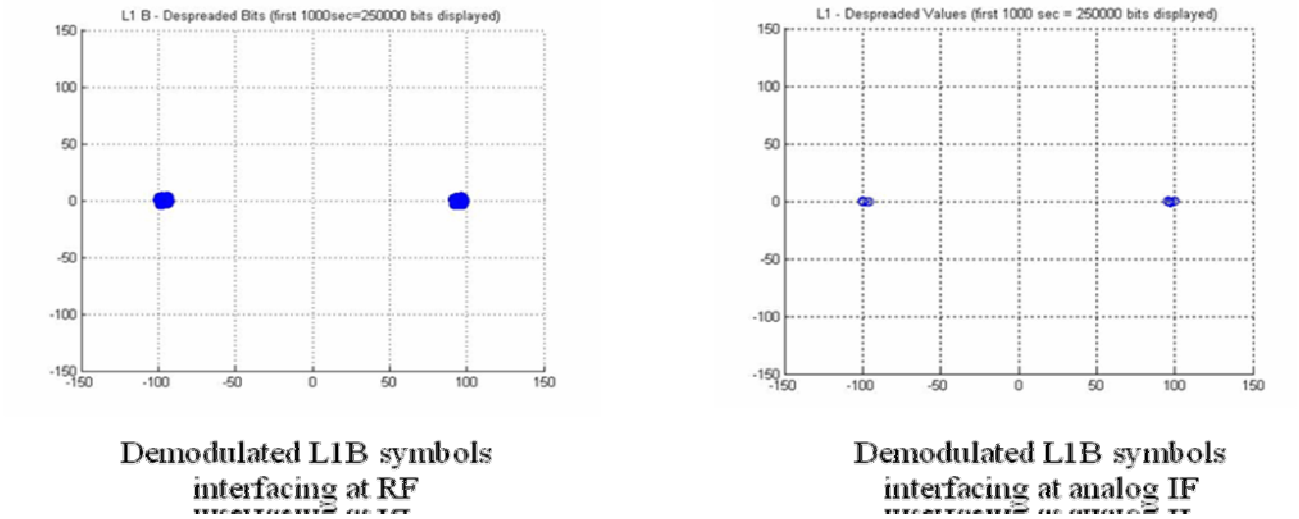

Fig. 8

Finally the GUI and Timing Receiver interact to provide log files of the demodulated message pages. Below in Fig. 9 we report the L1B Navigation Monitor file report elaborated by the Timing Receiver GUI when the Receiver is tracking in real time.

All the L1B message fields are decoded and reported as they are demodulated by the RF and Base Band receiver front ends.

Space Technology S.r.l.
Piazza Augusto Righi N. 8
(00146) Rome Italy
Contact: sales@spacetechnology.it
Phone: +39-06-55133935

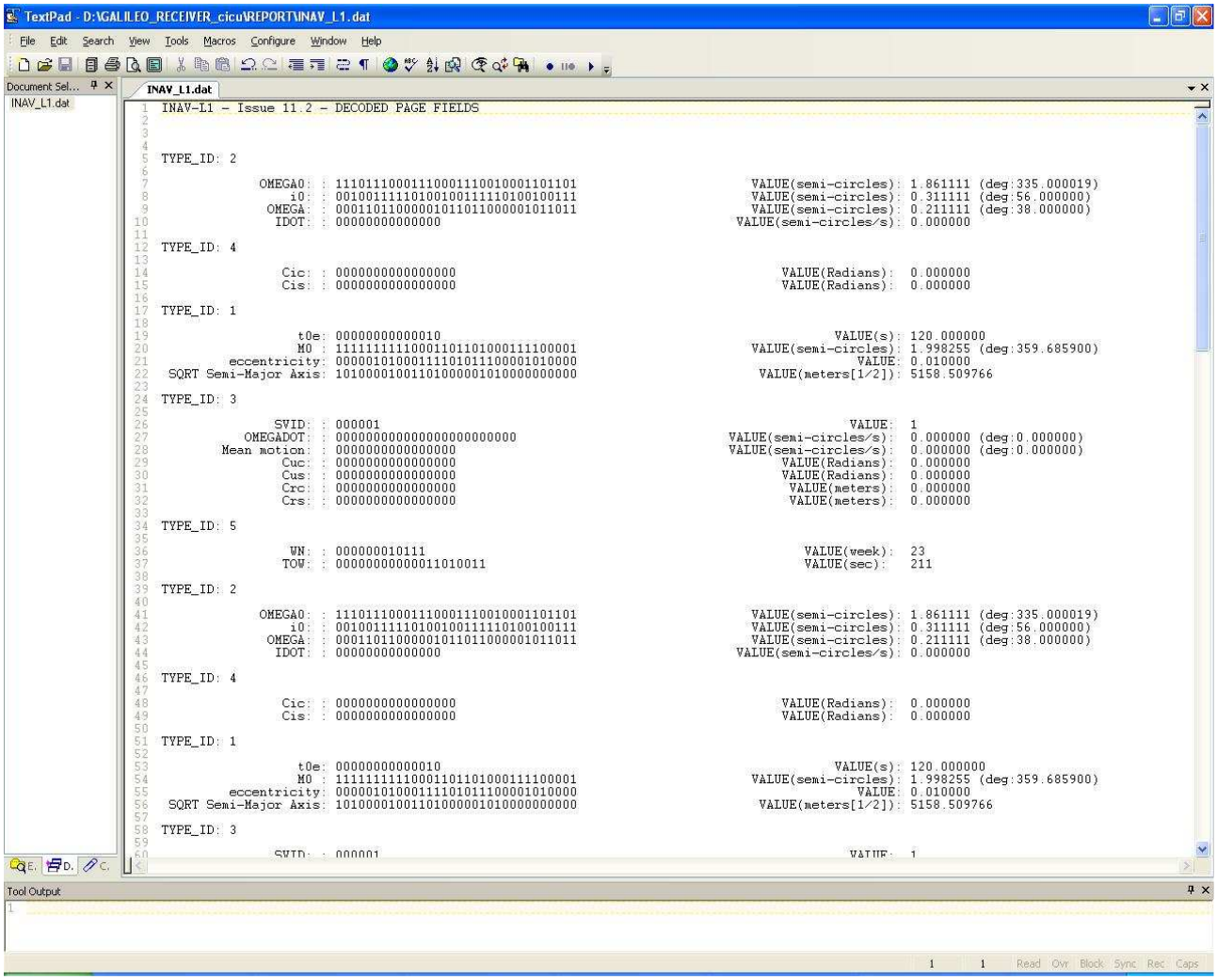

Fig. 9

Space Technology S.r.l.
Piazza Augusto Righi N. 8
(00146) Rome Italy
Contact: sales@spacetechnology.it
Phone: +39-06-55133935